

**PRELIMINARY**

**DESCRIPTION:**

The DPS512X24MFn3 High Speed SRAM "STACK" modules are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC). Available in straight leaded, "J" leaded or gullwing leaded packages. The module packs 12-Megabits of low-power CMOS static RAM in an area as small as 0.549 in<sup>2</sup>, while maintaining a total height as low as 0.200 inches.

The DPS512X24MFn3 STACK modules contain three individual 512K x 8 SRAMs, each packaged in a hermetically sealed SLCC, making the modules suitable for commercial, industrial and military applications.

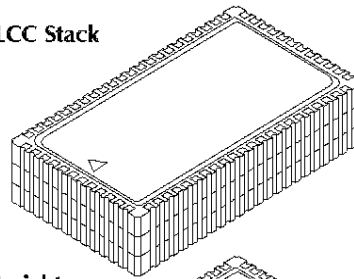
By using SLCCs, the "Stack" family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

**FEATURES:**

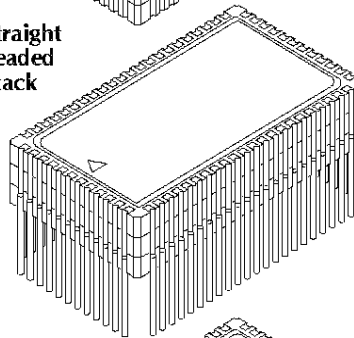
- Organizations Available:
  - 512K x 24 or 1.5 Meg x 8
- Access Times: 20\*, 25, 30, 35, 45ns
- Fully Static Operation
  - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Packages Available:
  - SLCC Stack
  - Straight Leaded Stack
  - "J" Leaded Stack
  - Gullwing Leaded Stack

\* Commercial and Industrial Grade only.

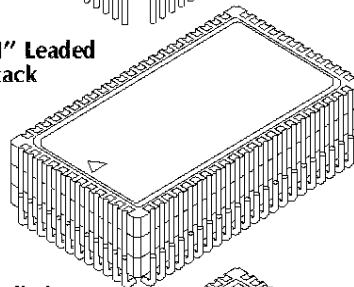
**SLCC Stack**



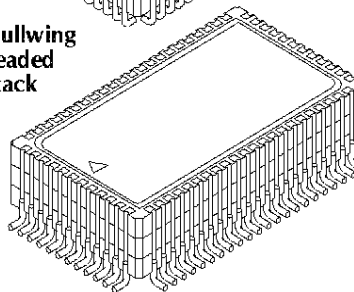
**Straight Leaded Stack**



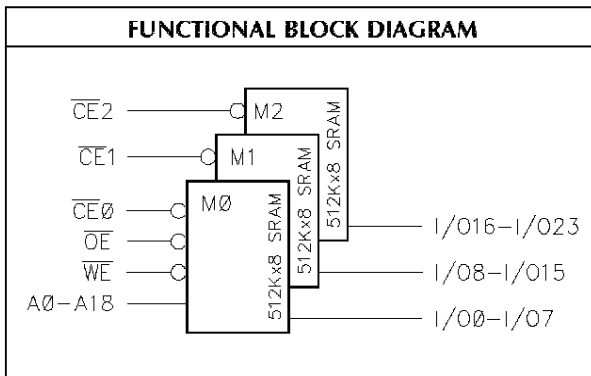
**"J" Leaded Stack**



**Gullwing Leaded Stack**



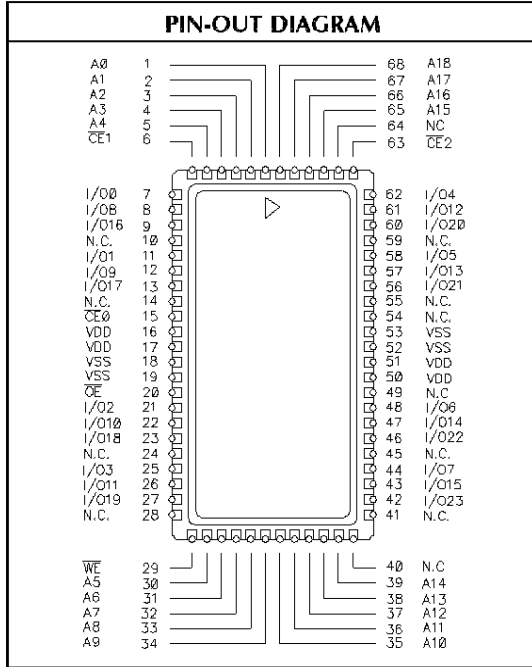
**FUNCTIONAL BLOCK DIAGRAM**



**PIN NAMES**

PIN NAMES	
A0 - A18	Address Inputs
I/O0 - I/O23	Data Input/Output
CE0 - CE2	Low Chip Enables
WE	Write Enable
OE	Output Enable
V <sub>DD</sub>	Power (+5V)
V <sub>SS</sub>	Ground
N.C.	No Connect

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Mode	CE	WE	OE	I/O Pin	Supply Current
Not Selected	H	X	X	High-Z	Standby
D <sub>OUT</sub> Disable	L	H	H	High-Z	Active
Read	L	H	L	D <sub>OUT</sub>	Active
Write	L	L	X	D <sub>IN</sub>	Active

H = HIGH L = LOW X = Don't Care

Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V <sub>DD</sub>	Supply Voltage	4.5	5.0	5.5	V	
V <sub>IH</sub>	Input HIGH Voltage	2.2		V <sub>DD</sub> +0.3	V	
V <sub>IL</sub>	Input LOW Voltage	-0.5 <sup>2</sup>		0.8	V	
T <sub>A</sub>	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

Symbol	Parameter	Max.	Unit	Condition
C <sub>ADR</sub>	Address Input	30	pF	V <sub>IN</sub> <sup>2</sup> = 0V
C <sub>CE</sub>	Chip Enable	16		
C <sub>WE</sub>	Write Enable	30		
C <sub>OE</sub>	Output Enable	30		
C <sub>I/O</sub>	Data Input/Output	16		

Symbol	Parameter	Value	Unit
T <sub>STC</sub>	Storage Temperature	-65 to +150	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
V <sub>DD</sub>	Supply Voltage <sup>1</sup>	-0.5 to +7.0	°C
V <sub>IO</sub>	Input/Output Voltage <sup>1</sup>	-0.5 to V <sub>DD</sub> +0.5	V

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>OH</sub>	HIGH Voltage	I <sub>OH</sub> = -4.0mA	2.4		V
V <sub>OL</sub>	LOW Voltage	I <sub>OL</sub> = 8.0mA		0.4	V

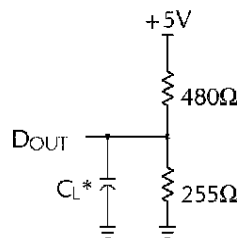
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>DD</sub>	-	-15	+15	-15	+15	-15	+15	µA
I <sub>OUT</sub>	Output Leakage Current	V <sub>IO</sub> = 0V to V <sub>DD</sub> , CE or OE = V <sub>IH</sub> , or WE = V <sub>IL</sub>	-	-10	+10	-10	+10	-10	+10	µA
I <sub>CC</sub>	Operating Supply Current	Cycle = min., Duty = 100% I <sub>OUT</sub> = 0mA	x8	165	290	300	300	300	300	mA
			x24	375	510	540	540	540		
I <sub>SB1</sub>	Full Standby Supply Current	V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V or V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V	3	30	30	45	45	45	45	mA
I <sub>SB2</sub>	Standby Current (TTL)	CE = V <sub>IH</sub>	60	180	180	180	180	180		
I <sub>DR3</sub>	Data Retention Supply Current (3.0V)	V <sub>DR</sub> = 3.0V, CE ≥ V <sub>DR</sub> - 0.2V	0.45	1.5	3.0	6.0	6.0	6.0	6.0	mA
I <sub>DR2</sub>	Data Retention Supply Current (2.0V)	V <sub>DR</sub> = 2.0V, CE ≥ V <sub>DR</sub> - 0.2V	0.3	0.9	2.4	5.4	5.4	5.4		
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> = 8.0mA	-	0.4	0.4	0.4	0.4	0.4	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = -4.0mA	-	2.4	2.4	2.4	2.4	2.4		

† Typical measurements made at +25°C, Cycle = min., V<sub>DD</sub> = 5.0V.

## PRELIMINARY

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

Figure 1. Output Load



OUTPUT LOAD		
Load	CL	Parameters Measured
1	100pF	except tLZ, tHZ, tOHZ, tOLZ, and tWHZ
2	5pF	tLZ, tHZ, tOHZ, tOLZ, and tWHZ

Data Retention AC Characteristics <sup>8</sup>						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	$\overline{CE} \geq V_{DR} - 0.2V$	2.0	-	-	V
V <sub>CDR</sub>	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t <sub>R</sub>	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

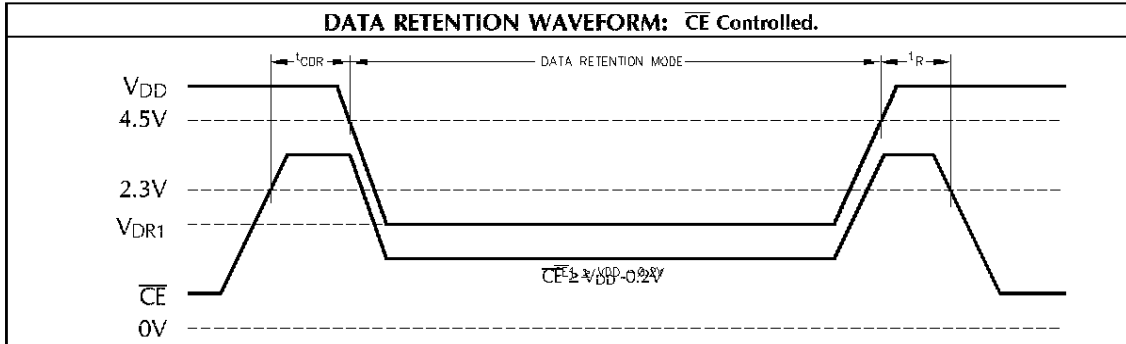
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t <sub>RC</sub>	Read Cycle Time	20		25		30		35		45		ns
2	t <sub>AA</sub>	Address Access Time		20		25		30		35		45	ns
3	t <sub>CO</sub>	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t <sub>OE</sub>	Output Enable to Output Valid		10		12		15		20		25	ns
5	t <sub>LZ</sub>	$\overline{CE}$ to Output in LOW-Z <sup>4,5</sup>	3		3		3		3		3		ns
6	t <sub>OLZ</sub>	Output Enable to Output in LOW-Z <sup>4,5</sup>	0		0		0		0		0		ns
7	t <sub>HZ</sub>	$\overline{CE}$ to Output in HIGH-Z <sup>4,5</sup>		8		10		15		20		25	ns
8	t <sub>OHZ</sub>	Output Enable to Output in HIGH-Z <sup>4,5</sup>	0	8	0	10	0	15	0	20	0	25	ns
9	t <sub>OH</sub>	Output Hold from Address Change	4		5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE <sup>6,7</sup> : Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t <sub>WC</sub>	Write Cycle Time	20		25		30		35		45		ns
11	t <sub>AW</sub>	Address Valid to End of Write	13		15		20		25		35		ns
12	t <sub>CW</sub>	Chip Enable to End of Write	13		15		20		25		35		ns
13	t <sub>AS</sub>	Address Set-Up Time **	0		0		0		0		0		ns
14	t <sub>WP</sub>	Write Pulse Width	13		15		20		25		35		ns
15	t <sub>WR</sub>	Write Recovery Time	0		0		0		0		0		ns
16	t <sub>WHZ</sub>	Write Enable to Output in HIGH-Z <sup>4,5</sup>	0	8	0	10	0	12	0	15	0	20	ns
17	t <sub>DW</sub>	Data to Write Time Overlap	9		10		12		15		20		ns
18	t <sub>DH</sub>	Data Hold from Write Time	0		0		0		0		0		ns
19	t <sub>OW</sub>	Output Active from End of Write	3		3		3		3		3		ns

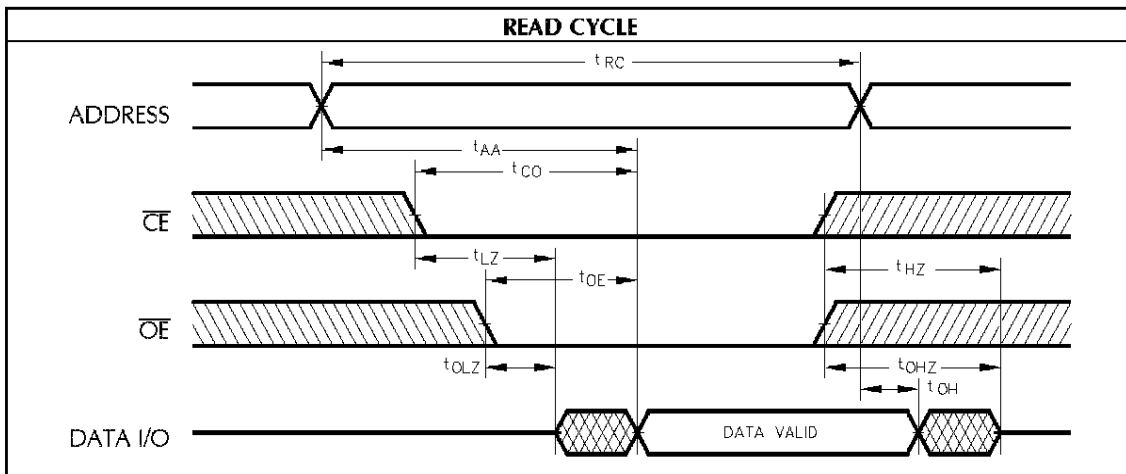
\* Available in Commercial and Industrial Grade Only.

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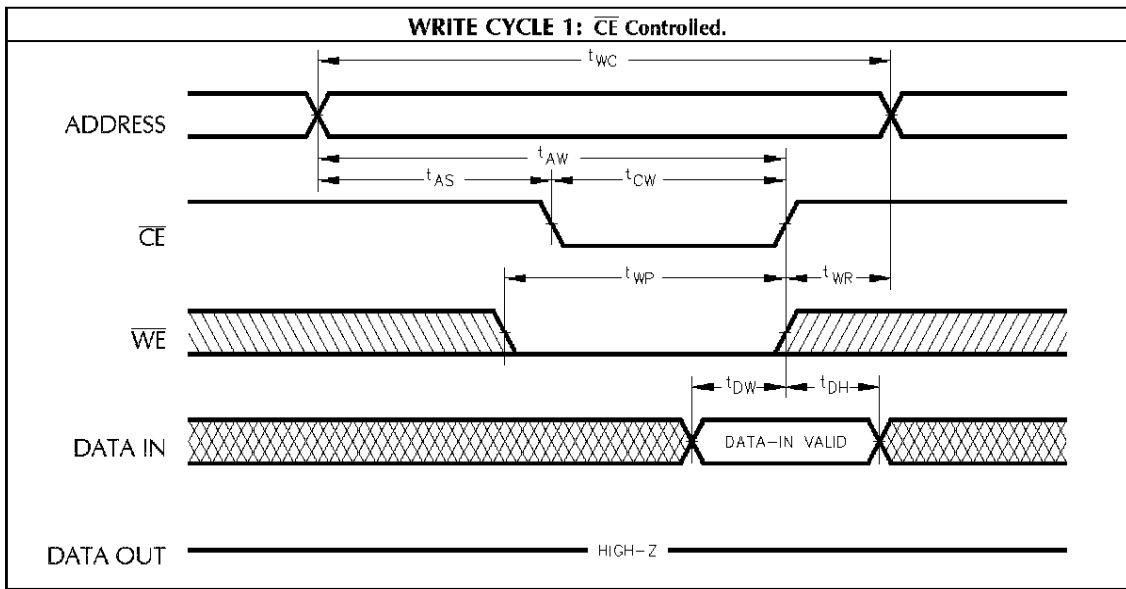
DATA RETENTION WAVEFORM:  $\overline{CE}$  Controlled.



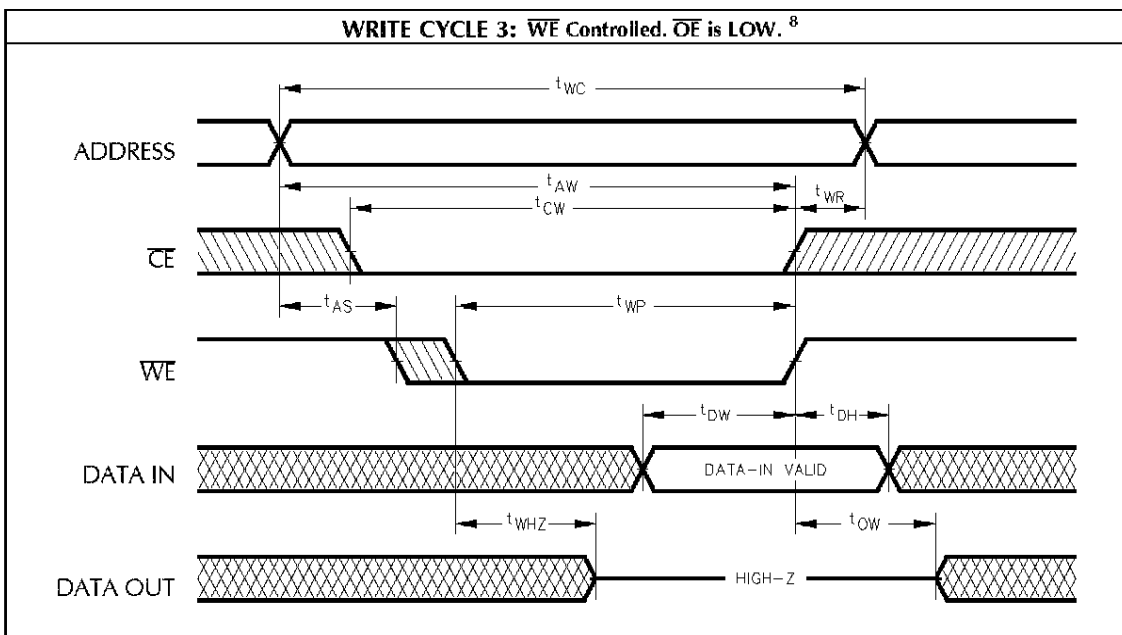
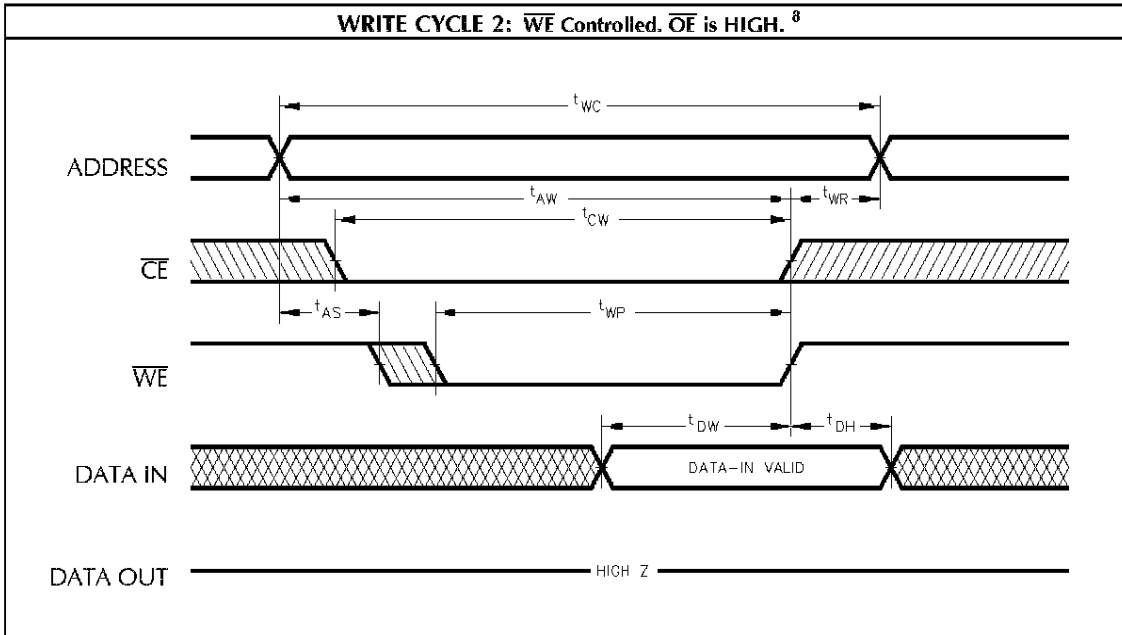
READ CYCLE



WRITE CYCLE 1:  $\overline{CE}$  Controlled.

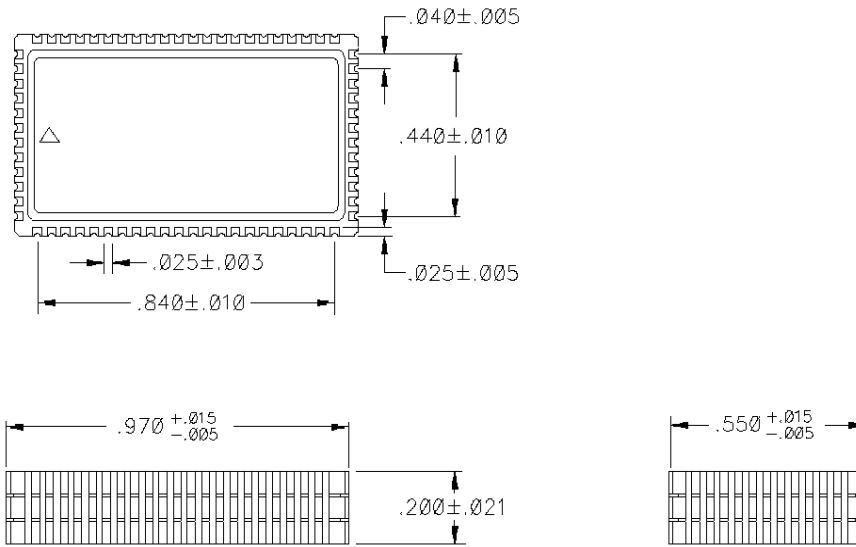


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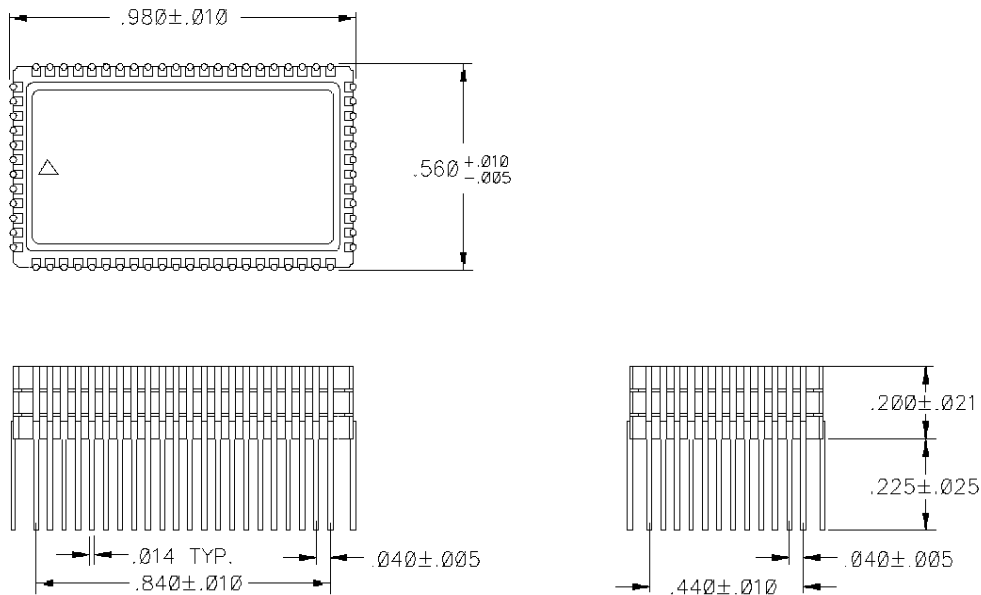


PRELIMINARY

(68 - PIN LEADLESS STACK) MECHANICAL DRAWING

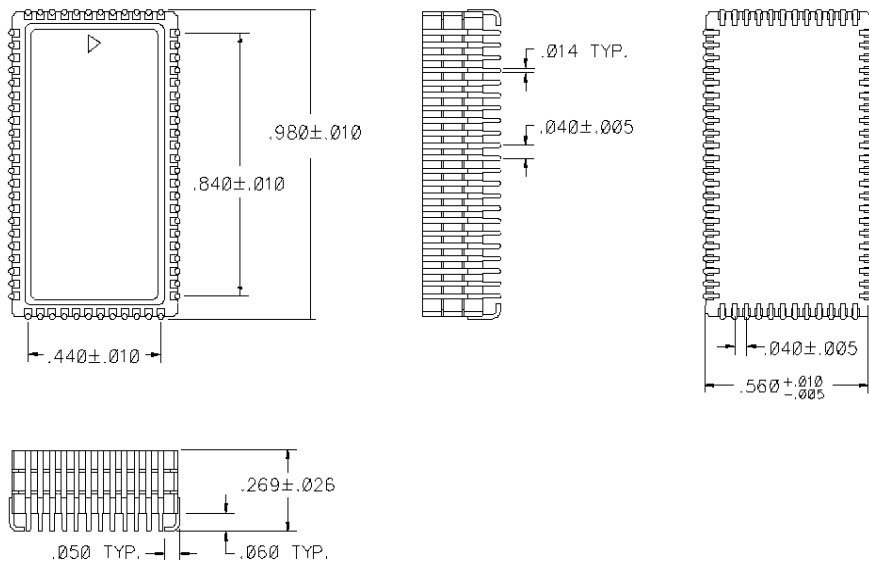


(68 - PIN STRAIGHT LEADED STACK) MECHANICAL DRAWING

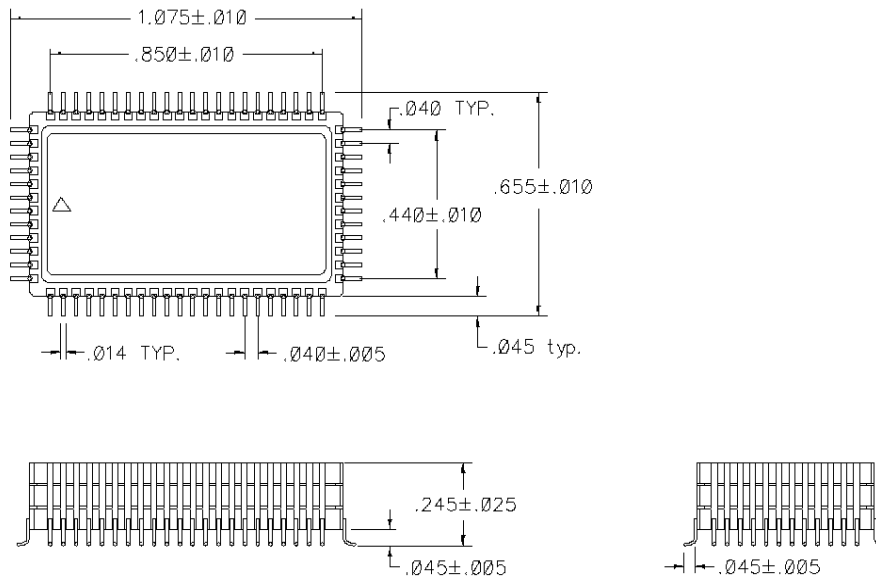


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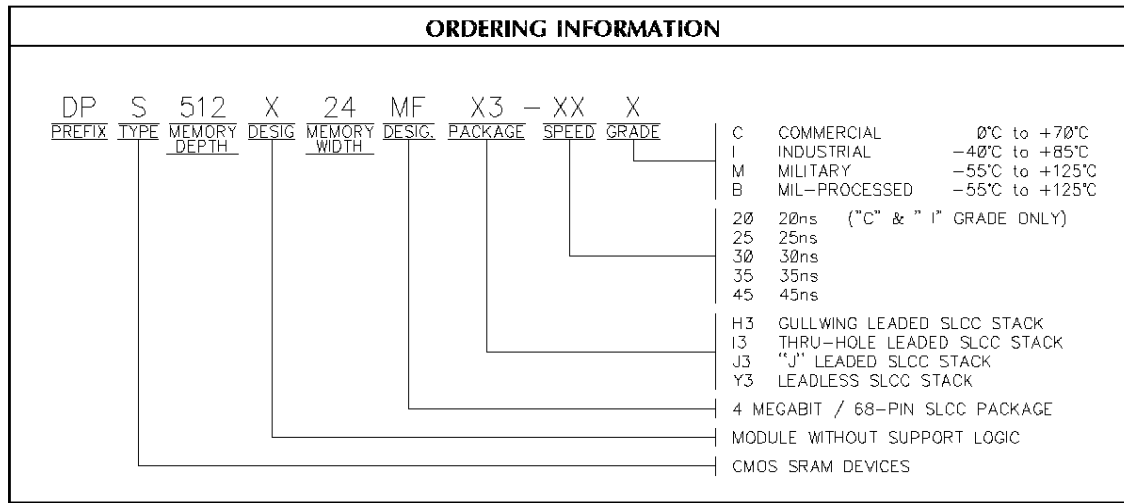
(68 - PIN "J" LEADED STACK) MECHANICAL DRAWING



(68 - PIN GULLWING LEADED STACK) MECHANICAL DRAWING

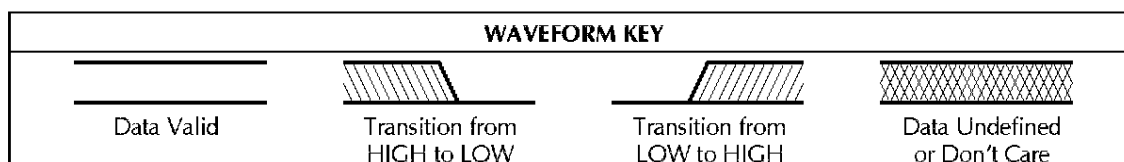


PRELIMINARY



**NOTES:**

1. All voltages are with respect to V<sub>SS</sub>.
2. -2.0V min. for pulse width less than 20ns (V<sub>IL</sub> min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when  $\overline{WE}$  is LOW.
8.  $\overline{CE}$  and  $\overline{WE}$  can initiate and terminate WRITE Cycle.



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